WHAT IS CLAIMED IS:

1. A trench field effect transistor formed on a silicon substrate, the trench transistor comprising:

a trench extending into the substrate;

a dielectric layer formed on walls and bottom of the trench; and

a gate conductive material substantially filling the trench,

wherein, the dielectric layer comprises a gate oxide layer grown at a temperature above about 1,100 °C to result in the gate oxide layer having a thickness that is substantially uniform, the gate oxide layer having substantially uniform stress.

2. The trench transistor of claim 1 wherein the dielectric layer further comprises:

a silicon nitride layer disposed on the gate oxide layer; and

a second oxide layer disposed between the silicon nitride layer and the gate conductive material.

3. The trench transistor of claim 2 wherein the gate oxide layer has a first thickness of at least about 300 Å, the silicon nitride layer has a second thickness of about 120Å, and the second oxide layer has a third thickness of about 50 Å.

4. A trench field effect transistor formed on a silicon substrate, the trench transistor comprising:

a trench extending into the substrate;

a first oxide layer thermally grown on walls and bottom of the trench;

a silicon nitride layer disposed on the first oxide layer;
a second oxide layer disposed on the silicon nitride layer; and
a gate conductive material substantially filling the trench.

5. The trench transistor of claim 4 wherein the first oxide layer is grown at a temperature of at least about 1,100°C.

6. The trench transistor of claim 5 wherein the first oxide has a thickness of about 300Å.

7. The trench transistor of claim 6 wherein the silicon nitride layer has a thickness of about 120Å.

8. The trench transistor of claim 7 wherein the second oxide layer has a thickness of about 50Å.

9. A method of forming a gate dielectric layer of a trench field-effect transistor, the method comprising the steps of:
(a) forming a trench in silicon on a substrate; and
(b) heating the substrate to at least about 1,100 °C to form a layer of silicon oxide at least about 100 Å thick inside the trench.

10. The method of claim 9 further comprising the steps of:
(c) forming a layer of silicon nitride on the layer of silicon oxide; and
(d) forming a second layer of oxide on the layer of silicon nitride.

11. The method of claim 10 wherein the layer of silicon nitride is about 120Å thick.

12. The method of claim 10 wherein a low-pressure chemical-vapor deposition process is used to form a conformal layer of silicon nitride.

13. The method of claim 11 wherein the second layer of oxide is about 50Å thick.

14. A method of forming a gate dielectric layer of a trench field-effect transistor, the method comprising:

(a) forming a trench in silicon on a substrate;

(b) heating the substrate to at least about 1,100 °C to form a layer of silicon oxide at least about 100Å thick;

(c) forming a conformal layer of silicon nitride about 120Å thick on the layer of silicon oxide by a low-pressure chemical-vapor deposition process; and

(d) growing a second layer of oxide about 50Å thick on the layer of silicon nitride.